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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,486	09/02/2003	Yuji Sano	122.1566	2761

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EXAMINER	
BECK, ALEXANDER S	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/652,486	SANO ET AL.	
	Examiner	Art Unit	
	Alexander S. Beck	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-34 and 37-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-34 and 37-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 30, 2007, has been entered, in which: claims 31 and 37 are amended; claims 35 and 36 are cancelled; and the rejections of the claims are traversed.

Claim Rejections - 35 USC § 112

2. The rejection of claims 31-36 and 38-39 set forth in paragraphs 1-3 of the final Office action mailed on January 30, 2007, are withdrawn in light of applicant's cancellation of claims 35 and 26.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 31-34, 38 and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 7,034,468 to Kim et al. (hereinafter "Kim").

As to claim 31, Kim discloses a plasma display apparatus in Figures 1-3 comprising: a plasma display panel having at least a pair of electrodes making up a capacitive load (10) and causing discharge to occur between the pair of electrodes; and a capacitive load drive circuit (100) connected to a respective electrode of the pair of electrodes and driving the capacitive load (10). (Kim at col. 3, ll. 48-61.) The capacitive load drive circuit has a coil circuit (C_{SS}, 120, 130, L, C_S) connected between an output terminal to be connected to said respective electrode (i.e. node connecting SW4 with C_S) and a reference potential (V_{SS}) and controls so that when the energy stored in the capacitive load (10) is discharged, the energy stored in the coil circuit (C_{SS}, 120, 130, L, C_S) and at the same time the energy retained in the coil circuit (C_{SS}, 120, 130, L, C_S) while the current flowing through the coil circuit (C_{SS}, 120, 130, L, C_S) is increasing, and when the capacitive load (10) is recharged, the stored energy is released while the current flowing through the coil circuit (C_{SS}, 120, 130, L, C_S) is decreasing. (Kim at col. 3, ln. 62 – col. 4, ln. 34.) As one of ordinary skill in the art would appreciate, the above features are inherent to a LC resonant circuit process.

Moreover, Kim discloses wherein the energy is stored in the coil circuit (C_{SS}, 120, 130, L, C_S) via said respective electrode when the energy stored in the capacitive load (10) is discharged and the released energy is supplied to the capacitive load (10) via the respective electrode when the capacitive load (10) is recharged. (Kim at col. 3, ln. 62 – col. 4, ln. 34.) As one of ordinary skill in the art would appreciate, this is achieved since these are the respective electrodes that define/possess the capacitive load.

As to claim 32, Kim discloses wherein a switch circuit (SW5) maintaining the discharged state of the capacitive load (10) after the capacitive load (10) is discharged and until it is recharged, and a power supply switch circuit (SW4) maintaining the charged state of the capacitive load (10) after the capacitive load (10) is charged and until it is discharged again. (Kim at col. 3, ln. 62 – col. 4, ln. 34.)

As to claim 33, Kim discloses wherein the switch circuit (SW5) is comprised of a one-way conductive element (e.g. diode). As can be seen from the embodiment in Figures 4 and 6, the switching circuits maintaining the discharge state, and controlled by T6 and T4 respectively, include diodes.

As to claim 34, Kim discloses wherein the power supply switch circuit (SW4) is controlled so as to be brought into a conductive state before the charging of the capacitive load (10) is completed. For example, and as can be seen in Figure 3, none of the charging can occur before bringing switch SW4 into a conductive state since the power supplying the charge would be disconnected.

As to claim 38, Kim discloses wherein the capacitive load drive circuit (100) further comprises: a first switch (SW4) connected in series between an output terminal to be connected to said respective electrode (i.e. node connecting SW5 with 10) and one end of the coil circuit (C_{SS}, 120, 130, L, C_S); a second switch circuit (SW1) connected between a first end of the coil circuit (e.g. node connecting SW1 with coil circuit C_{SS}, 120, 130, L, C_S) and the reference potential (V_{SS}); a third switch circuit (SW1) connected between a second end of the coil circuit (e.g. also reads on node connecting SW1 with coil circuit C_{SS}, 120, 130, L, C_S) and the reference potential (V_{SS}); wherein the first (SW4), second (SW1), and third (SW1) switches are controlled

to store energy in the coil circuit (C_{SS}, 120, 130, L, C_S) and to release the stored energy from the coil circuit (C_{SS}, 120, 130, L, C_S). (Kim at col. 3, ln. 62 – col. 4, ln. 34.)

As to claim 39, Kim discloses wherein the capacitive load drive circuit (100) further comprises a fourth switch circuit (SW2, SW3) connected between the second end of the coil circuit (C_{SS}, 120, 130, L, C_S) and the output terminal (i.e. node connecting SW5 with 10). (Kim at col. 3, ln. 62 – col. 4, ln. 34.)

5. Claims 31 and 37-39 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,922,180 to Iwami et al. (hereinafter "Iwami").

As to claim 31, Iwami discloses a plasma display apparatus in Figure 5 comprising: a plasma display panel having at least a pair of electrodes making up a capacitive load (e.g. Y_j, X_j, D_i) and causing discharge to occur between the pair of electrodes; and a capacitive load drive circuit (2, 3, 4) connected to a respective electrode of the pair of electrodes and driving the capacitive load. (Iwami at col. 8, ll. 1-12.) The capacitive load drive circuit has a coil circuit (e.g. any one of L1, D1, L2, D2, C1 or L3, D3, L4, D4, C4 or L5, D7, L6, D8, C3) connected between an output terminal to be connected to said respective electrode (e.g. any one of 11 or 13 or 15, respectively) and a reference potential (e.g. any one of B1 or B3 or B7, respectively) and controls so that when the energy stored in the capacitive load is discharged, the energy stored in the coil circuit and at the same time the energy retained in the coil circuit while the current flowing through the coil circuit is increasing, and when the capacitive load is recharged, the stored energy is released while the current flowing through the coil circuit is decreasing. (Iwami at col. 5, ll. 27-38; col. 5, ln. 57 – col. 6, ln. 23; col. 8, ll. 24-30; col. 11, ll. 32-41.)

Moreover, Iwami discloses wherein the energy is stored in the coil circuit via said respective electrode when the energy stored in the capacitive load is discharged and the released energy is supplied to the capacitive load via the respective electrode when the capacitive load is recharged. (Iwami at col. 5, ll. 27-38; col. 5, ln. 57 – col. 6, ln. 23.)

As to claim 37, Iwami discloses wherein the pair of electrodes are a plurality of scan electrodes (e.g. Y_j, X_j) and a plurality of address electrodes (e.g. D_i) arranged so as to intersect the scan electrodes. (Iwami at Figure 5.) The capacitive load drive circuit (2, 3, 4) comprises: a scan electrode drive circuit (3, 4) driving the plurality of scan electrodes; and an address electrode drive circuit (2) driving the plurality of address electrodes, wherein the address electrode drive circuit has a coil circuit (e.g. L5, D7, L6, D8, C3) connected between an output terminal to be connected to the address electrode (e.g. 15) and a reference potential (e.g. B7) and controls so that when the energy stored in the capacitive load consisting of the address electrodes and the scan electrodes is discharged, the energy is stored in the coil circuit and at the same time the energy is retained in the coil circuit while the current flowing through the coil circuit is increasing, and when the capacitive load is recharged, the stored energy is released while the current flowing through the coil circuit is decreasing. (Iwami at col. 8, ln. 30 – col. 9, ln. 20.)

As to claim 38, Iwami discloses wherein the capacitive load drive circuit further comprises: a first switch circuit (S11) connected in series between an output terminal to be connected to said respective electrode (e.g. 13) and one end of the coil circuit (e.g. output of D3 of coil circuit L3, D3, L4, D4, C4); a second switch circuit (S14) connected between a first end of the coil circuit (e.g. input of L4) and the reference potential (B3); a third switch circuit (S13) connected between a second end of the coil circuit (e.g. output of D3) and the reference potential

(B3); wherein the first, second, and third switches are controlled to store energy in the coil circuit and to release the stored energy from the coil circuit. (Iwami at col. 5, ln. 57 – col. 6, ln. 23.)

As to claim 39, Iwami discloses wherein the capacitive load drive circuit further comprises a fourth switch circuit (S15) connected between the second end of the coil circuit (e.g. output of D3) and the output terminal (e.g. 13). (Iwami at col. 5, ln. 57 – col. 6, ln. 23.)

Response to Arguments

6. Applicant's arguments with respect to claims 31-34 and 37-39 have been considered but are moot in view of the new grounds of rejection. For example, the LC circuits of Kim and Iwami has been interpreted to read on the claimed limitation "coil circuit".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander S. Beck whose telephone number is (571) 272-7765. The examiner can normally be reached on M-F, 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alexander S. Beck
July 5, 2007

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER